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09/824,898	04/02/2001	Eric B. Kushnick	CRED 2164	2197

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	5

DATE MAILED: 08/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/824,898	KUSHNICK, ERIC B.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment A dated June 7, 2004.

2. Claims 1-38 are presented for examination.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Re Claims 1-8, 11,15-16,20-27, 30, and 34-35

4. Claims 1-8, 11, 15-16, 20-27, 30, and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heyne, U.S. Patent 6194928, in view of Hondeghem, U.S. Patent 4255790.

5. In re claim 1, Heyne discloses an apparatus [delay unit T] for generating pulses of a third pulse sequence [OUT] in response to pulses of a periodic first pulse sequence [IN] having a period Tp, wherein timing of each pulse of the third pulse sequence is adjustable with a resolution that is smaller than period Tp [fig.1; summary of invention; adjustment resolution of delays have to be less than Tp in order to "incrementally" adjust until desired delay is reached], the apparatus comprising:

- First means [delay elements I1 with mux1] to generate each second pulse [output from mux1] in response to a separate pulse of the first pulse sequence with a first delay adjustable by a first control data [first control line 1] and a resolution of Tp/N [t1] over a first range [12t1] substantially wider than Tp/M [t2], wherein M [5] and N [12] are

differing integers greater than one [fig.3; col.3, l.41 – col.4, l.38; 12t1 == 3t2 where 12t1 is wider than t2].

- Second means [delay elements I2 with mux2] to generate each third pulse in response to a separate pulse of the second pulse sequence with a delay adjustable by a second control data [second control line 2] with a resolution of Tp/M [t2] over a second range [5t2] substantially wider than Tp/N [t1] [fig.3; col.3, l.41-col.4, l.38; 5t2 is wider than t1].
- A programmable sequencer [control unit CTR and phase detector; CTR is programmable with up/down controls from phase detector and in the broadest sense, programmed relating to the sequence of steps depicted in fig.3 to arrive at the appropriate configuration of delay elements] for changing a magnitude of the first control data and a magnitude of the second control data [control driven by CTR to each mux in determining the number of delay elements to be utilized represents the magnitude for each respective means] in response to each pulse of the first pulse sequence [phase detector generates up/down control to CTR in response to first pulse IN] such that the magnitudes of the first and second control data vary in a programmably adjustable manner [fig.1-3; col.4, l.39 – col.5, l.21].

6. Hayne did not disclose that the programmable sequencer may vary the magnitudes in a repetitive fashion.

7. Hondeghem discloses an apparatus [fig.1] for generating pulses of a pulse sequence [A1-E1] in response to pulses of a periodic first pulse sequence [76] having a period Tp [abstract], the apparatus comprising:

- A programmable sequencer [CPU 70, RAM 84, I/O logic 112 with other associated circuitries] for changing a magnitude of the first control data [116] and a magnitude of the second control data [118] in response to each pulse of the first pulse sequence [76] such that the magnitudes of the first and second control data vary *repetitively* in a programmably adjustable manner [fig.2-3; col.4, l.62 – col.5, l.57; col.6, ll.20-57; program X# of times for desired repetition].

8. It would have been obvious to one of ordinary skill in the art, having the teachings of Hayne and Hondeghem before him at the time the invention was made, to modify the apparatus discloses by Hayne to include the programmable sequencer disclosed by Hondeghem, in order to obtain the programmable sequencer for changing a magnitude of the first control data and a magnitude of the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control data vary *repetitively* in a programmably adjustable manner. One of ordinary skill in the art would have been motivated to make such a combination in order to provide a way for performing tests that require various programmable repetitive sequences of pulse generation [col.1, ll.26-62].

9. As per claims 2 and 5, Heyne discloses M [5] and N [12] to be relatively prime [fig.3; 5 and 12 have common factor of 1].

10. As per claim 3, Heyne discloses at least one of the first and second ranges to be wider than Tp [abstract; fig.1-3; the second delay unit comprises of coarse delay elements that are used initially to increment the delay time to the range of the desired delay period, when the desired delay period is exceeded, a coarse delay element is removed and subsequent adjustments are performed with the first delay unit with finer delay elements, ergo, an ordinary artisan would

have inferred that the second delay unit must be designed with a range wider than the expected Tp in order for the initial adjustment to be performed correctly].

11. As per claim 4, Heyne discloses the first range is at least as wide as (1-1/N)Tp and the second range is at least as wide as (1-1/M)Tp [abstract; fig.1-3; both delay circuits have at least Tp and 5/3 Tp ranges, respectively, since Tp/N and Tp/M are integer fractions].

12. As per claim 6, Heyne discloses the generated third pulse sequence to be periodic [col.2, ll. 4-5].

13. As per claim 7, Heyne discloses a plurality of first gates [inverters or delay elements I1] connected in series for generating second pulses in response to first pulses wherein each first gate has a switching delay of Tp/N [fig.1; col.3, l.50].

14. As per claim 8, Heyne discloses a plurality of second gates [inverters or delay elements I2] connected in series for generating third pulses in response to second pulses wherein each second gate has a switching delay of Tp/M [fig.1; col.3, ll.51-52].

15. As per claims 11 and 16, Heyne discloses the apparatus wherein:

- The first means comprises a plurality of first gates [I1] connected in series for generating pulses of the second pulse sequence in response to first pulses wherein each first gate has a switching delay of Tp/N [fig.1; col.3, l.50].
- The second means comprises a plurality of second gates [I2] connected in series for generating pulses of the third pulse sequence in response to pulses of the second pulse sequence wherein each second gate has a switching delay of Tp/M [fig.2; col.3, ll.51-52].

16. In re claim 15, Heyne discloses an apparatus [delay unit T] for generating pulses of a third pulse sequence [OUT] in response to pulses of a periodic first pulse sequence [IN] having a

period Tp, wherein timing of each pulse of the third pulse sequence is adjustable with a resolution that is smaller than period Tp [fig.1; summary of invention; adjustment resolution of delays have to be less than Tp in order to "incrementally" adjust until desired delay is reached], the apparatus comprising:

- First means [delay elements I1 with mux1] to generate each second pulse [output from mux1] in response to a separate pulse of the first pulse sequence with a delay adjustable by a first control data [first control line 1] with a resolution of Tp/N [t1] [fig.3; col.3, l.41 – col.4, l.38].
- Second means [delay elements I2 with mux2] to generate each third pulse in response to a separate pulse of the second pulse sequence with a delay adjustable by a second control data [second control line 2] with a resolution of Tp/M [t2] [fig.3; col.3, l.41-col.4, l.38].
- A programmable sequencer [control unit CTR and phase detector; CTR is programmable with up/down controls from phase detector and in the broadest sense, programmed relating to the sequence of steps depicted in fig.3 to arrive at the appropriate configuration of delay elements] for changing a magnitude of the first control data and a magnitude of the second control data [control driven by CTR to each mux in determining the number of delay elements to be utilized represents the magnitude for each respective means] in response to each pulse of the first pulse sequence [phase detector generates up/down control to CTR in response to first pulse IN] such that the magnitudes of the first and second control data vary in a programmably adjustable manner [fig.1-3; col.4, l.39 – col.5, l.21].

17. Hayne did not disclose that the programmable sequencer may vary the magnitudes in a repetitive fashion.

18. Hondeghem discloses an apparatus [fig.1] for generating pulses of a pulse sequence [A1-E1] in response to pulses of a periodic first pulse sequence [76] having a period Tp [abstract], the apparatus comprising:

- A programmable sequencer [CPU 70, RAM 84, I/O logic 112 with other associated circuitries] for changing a magnitude of the first control data [116] and a magnitude of the second control data [118] in response to each pulse of the first pulse sequence [76] such that the magnitudes of the first and second control data vary *repetitively* in a programmably adjustable manner [fig.2-3; col.4, l.62 – col.5, l.57; col.6, ll.20-57; program X# of times for desired repetition].

19. It would have been obvious to one of ordinary skill in the art, having the teachings of Hayne and Hondeghem before him at the time the invention was made, to modify the apparatus discloses by Hayne to include the programmable sequencer disclosed by Hondeghem, in order to obtain the programmable sequencer for changing a magnitude of the first control data and a magnitude of the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control data vary *repetitively* in a programmably adjustable manner. One of ordinary skill in the art would have been motivated to make such a combination in order to provide a way for performing tests that require various programmable repetitive sequences of pulse generation [col.1, ll.26-62].

20. In re claims 20-27, 30, and 34-35, Heyne and Hondeghem disclose apparatus; therefore, Heyne and Hondeghem disclose method of operating apparatus.

Re Claims 9-10, 12-14, 17-19, 28-29, 31-33, and 36-38

21. Claims 9-10, 12-14, 17-19, 28-29, 31-33, and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heyne and Hondeghem as applied to claims 8 and 11 above, and further in view of Liedberg, U.S. Patent 5471165.

22. Heyne and Hondeghem disclose each and every limitation of the claims as discussed above in reference to claims 8 and 11. In particular, Heyne discloses an integrated pulse delay device comprising of two delay units wherein the units comprises of gates connected in series for generating a range of delay periods that can be monitored to produce the appropriate control signals for phase-locking the first input and final output pulses [fig.2].

23. However, Heyne and Hondeghem did not disclose an extra series of gates for the delay units or a way to monitor and phase-lock the first input pulse sequence with the output pulse sequence from the first gates.

24. Liedberg taught a modular signal processing circuit with means to delay a periodic input signal by utilizing a multitude of delay gates and means to monitor and phase-lock the input and output pulses [fig.2; col.4, ll.5-35].

25. In re claims 9, 12, and 17, Liedberg taught the modular pulse delay unit comprising of:

- M third gates [delay device D2] connected in series with second gates [delay device D1] for generating a fourth pulse sequence in delayed response to the first pulse sequence [fig.2; col.3, ll.57-58; col.4, ll.29-35].
- Wherein each second and third gate has a similar switching delay of Tp/M set by the magnitude of a second control signal applied to all the second and third gates [col.4, ll. 24-35; col.5, ll.31-40].

26. An ordinary artisan at the same time the invention was made would have been motivated to look for a way to increase the resolution and accuracy of a pulse delay generating device [Liedberg: col.1, ll.24-28; col.2, ll.48-54, ll.63-64].

27. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Heyne and Liedberg to provide a pulse delay generating device with a multitude of delay gates connected in series within a phase monitoring and locking system to increase the resolution and accuracy of the generated pulses.

28. As per claims 10, 13, and 18, Heyne taught the monitoring of a phase relationship between the first pulse sequence and the fourth pulse sequence and adjusting the magnitude of the first control signal so that the fourth pulse sequence is phase-locked with the first pulse sequence [fig. 2].

29. As per claims 14 and 19, Liedberg taught the modular pulse delay unit comprising of:

- Plurality of first N gates [delay device D1] connected in series for generating a pulse sequence in delayed response to the first pulse sequence [fig.2; col.3, ll.57-58; col.4, ll. 29-35].
- Wherein each gate has a switching delay set by the magnitude of a first control signal [col.4, ll.24-35; col.5, ll.31-40].
- Wherein the first pulse sequence and the generated pulse sequence are monitored and the first control signal is adjusted to phase lock the pulse sequences [col.4, ll.5-35].

30. As per claims 28-29, 31-33, and 36-38, Heyne, Hondeghem, and Liedberg taught apparatus; therefore, Heyne, Hondeghem, and Liedberg taught method of operating apparatus.

Response to Arguments

31. All limitations of claims as filed prior to Amendment dated June 7, 2004 not argued substantively in response filed as Amendment A dated June 7, 2004 are henceforth not applicable and the respective rejections are maintained.

32. Applicant's arguments with respect to claim 1, in regards to the amended portion of "a programmable sequencer for changing a magnitude of the first control data and a magnitude of the second control data in response to each pulse of the first pulse sequence such that the magnitudes of the first and second control data vary in a programmably adjustable manner" have been considered but are moot in view of the new ground(s) of rejection for all affected limitations as necessitated by amendment.

33. Applicant's arguments, with respect to claim 1 and other dependent claims argued in reference to "first and second delay circuits [having] delay resolutions that are fixed ratios of the period of the input signal IN" have been fully considered but they are not persuasive.

34. The Applicant correctly concedes that Heyne does teach adjustable delay circuits. The input period Tp is adjusted by the number of N or M delay elements [I1 or I2] to result in a resolution of Tp/N [t1] or Tp/M [t2]. Thus, according to the broadest interpretation, Heyne does satisfy the limitation of Tp/N and Tp/M resolutions as claimed in claim 1.

35. Alternately, it can also be demonstrated that Heyne also teaches or suggests Tp/N or Tp/M to be integer fractions of the period of an input signal.

36. Firstly, the Examiner specifically pointed to figure 3 in part 5 of the previous Office Action in regards to this limitation. The associated descriptions for figure 3 specifically point out that delay is adjusted so "that the phase of the output clock signal at the output OUT corresponds to the phase of the input clock CLK at the input IN" [col.4, ll.39-44]. Most importantly, figure 3

and its associated descriptions depict a simple illustration of how the phases are aligned ***incrementally*** with the adjustable delay circuits.

36. Secondly, simple mathematics would demonstrate that non-integer fractions would be very impractical to ***incrementally*** adjust to a whole [1/1.21 would take 121 parts to attain a whole number 100 without any remainders, in stark contrast to integer fraction ½ which would take just 2 parts to attain a whole number of 1].

37. Thirdly, Heyne's teachings pertain to the field of integrated circuits where processing speed is an important goal that obviously does not have to be stated. In the exception that Heyne was going against the conventional integrated circuit design goal, Heyne would have to disclose an advantage, a particular purpose, or solution to a stated problem for why the integrated circuit must be developed with design choices that would go against conventional standards. The Applicant can verify that Heyne did not disclose such contrary notions anywhere in the disclosure.

38. Therefore, one with ordinary skill in the art would have recognized that Heyne's apparatus is advocating the delay resolutions to be integer fractions of the period of an input signal in order to have a practical apparatus that can ***incrementally*** adjust the delay circuits to achieve synchronization.

39. Applicant's arguments, with respect to claim 2, in regards to "it is not possible for Heyne to teach or suggest that M and N are relatively prime" have been fully considered but they are not persuasive. The Examiner specifically pointed to figure 3 in the previous Office Action because figure 3 clearly shows that M and N are relatively prime [5 and 12 have common factor of 1].

40. Applicant's arguments, with respect to claim 4, in regards to the first delay circuit having a range that is at least as wide as (1-1/N)Tp, have been fully considered but they are not persuasive.

41. Claim 4 is essentially a definition of Heyne's invention according to the abstract that was pointed to by the Examiner in the previous Office Action. If there are to be N or M delay elements with Tp/N or Tp/M delay resolution, respectively, then each of the delay circuits in Heyne would have at least a range of Tp and 5/3Tp [second delay circuits is (5 * 4t1) with 12t1 being one Tp according to figure 3]. Denying this fact would go against the Applicant's arguments for Tp/N and Tp/M to be integer fractions of the input period Tp. The only disputable limitation concerning the range was that at least one of the first and second ranges had to be greater than Tp, which has been conceded by the Applicant.

42. Additionally, the Applicant's concession that "while Heyne does not directly teach that the second delay unit has a delay as large as Tp one of skill in the art would expect it to have a delay that large" is important because it demonstrates one of the important aspects of Heyne's invention: the second delay unit is used to initially increment the number of second delay elements close enough to the desired phase and then held constant. As the Examiner specifically pointed to the abstract which states "in the event of subsequent changes in the desired value or in the actual value, the number of ***first delay elements*** is incrementally altered, while the number of second delay elements in the signal path is kept ***constant***, the first delay circuit, thus, would have to have a range that is at least as wide as (1-1/N)Tp in order to properly adjust the delay after initialization since the second delay elements are held constant and can't be used in the event that a full period Tp adjustment is desired.

43. Applicant's arguments, with respect to claims 7 and 8, in regards to delays t1 and t2 of the first and second delay circuit gates I1 and I2, respectively, are some integer ratios of the delay of the IN signal, have been fully considered but they are not persuasive.

44. As discussed above in reference to response to argument to claim 1 in regard to the matter relating to integer fraction, t1 and t2 can be expected to be integer ratios [Tp/N or Tp/M] of the input signal.

45. Additionally, in response to applicant's argument that the reference fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., no provisions like the Applicant's "complicated circuitry" for ensuring that the delays of inverters are some integer fraction of the period of the IN signal) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). In short, even though Heyne does not disclose the "complicated circuitry" to ensure the delays of the inverters are some integer fraction of the period of the IN signal, it is not what the Applicant is claiming.

46. Applicant's arguments, with respect to claim 9, in regards to Liedberg not teaching "a delay circuit having the limitations of claim 9, such as the applicant's Fig.7, or illustrates the subject matter of claim 9", have been fully considered but they are not persuasive.

47. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

48. Additionally, it is noted that the features upon which applicant relies (i.e., gates 66 of Applicant's figure 7 are merely a part of the delay control mechanism for gates 60) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See discussion above pertaining to similar matter.

Conclusion

49. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
August 17, 2004

REHANA PERVEEN
PRIMARY EXAMINER